

REMARKS

This paper responds to the Office Action mailed on June 29, 2006.

None of the claims are amended. Claims 1-12, 17-47, and 66-75 are canceled without disclaimer or prejudice. Claims 76-78 are added. As a result, claims 13-16, 48-65, and 76-78 are now pending in this application.

Election to the Restriction Requirement

Restriction to one of the following claims was required:

- I. Claims 1-12, drawn to a device for repairing defects in a circuit, classified in class 714, subclass 718.
- II. Claims 13-16, 48-62 and 63-65, drawn to a device, system and method of testing an integrated circuit and repairing the memory using redundant memory, classified in class 714, subclass 710.
- III. Claims 17-47 and 66-75, drawn to embodiments of groups II and I, classified in class 714, subclass 718.

As provisionally elected by Applicant's representative, Viet V. Tong, on June 15, 2006, Applicant elects to prosecute the invention of Group II, claims 13-16 and 48-65.

The claims of the non-elected invention, claims 1-12, 17-47, and 66-75, are hereby canceled without disclaimer or prejudice. Applicant reserves the right to later file continuations or divisions having claims directed to the non-elected inventions.

§103 Rejection of the Claims

Claims 13-16 and 48-65 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Namekawa (U.S. 6,115,301).

Applicant respectfully traverses for at least the reasons presented below.

Objection to the Official Notice

The Office Action cites a single document (Namekawa) to reject claims 13-16 and 48-65 of the present application under 35 USC § 103(a) based on reasons that some of the specific

features in these claims, although not disclosed in the single document, are obvious arrangement of parts. Applicant assumes that the Examiner is taking Official Notice in rejecting these claims because the Office Action offers no documents to support the rejection of the specific features in these claims. Applicant respectfully traverses the taking of Official Notice and, pursuant to M.P.E.P. § 2144.03, Applicant requests documents or an affidavit to support the rejection. Moreover, Applicant cannot find in Namekawa a motivation to modify the teaching of Namekawa as proposed in the Office Action. In the absence of documents or an affidavit to support the rejection of claims 13-16 and 48-65, Applicant requests reconsideration, withdrawal of the rejection, and allowance of these claims. Notwithstanding the objection to the taking of Official Notice, Applicant believes that claims 13-16 and 48-65 are patentable over Namekawa for the reasons presented below.

Independent claim 13 recites, among other things, a plurality of switching units, each of the switching units is connected “in series with one of the memory segments between the second supply node and one of the internal nodes” and “each of the switching units includes an input node for receiving a select signal to electrically disconnect one of the memory segments from the second supply node based on a state of the select signal”.

Applicant believes that claim 13 is patentable over Namekawa because Applicant cannot find in Namekawa everything recited in claim 13.

The Office Action relies on FIG. 1 of Namekawa to reject claim 13. FIG. 1 of Namekawa teaches switches SW10 through SW115 and switches SW20 through SW215. The Office Action compares switches SW10 through SW115 and switches SW20 through SW215 to the switching units of claim 13. However, each of the switches SW10 through SW115 of Namekawa (e.g., SW10) is connected between a data line (e.g., DL0) and a data input/output lines (e.g., IO0). Similarly, each of the switches SW21 through SW215 of Namekawa (e.g., SW21) is also connected between a data line (e.g., DL0) and a data input/output line (e.g., IO1). Switch SW20 of Namekawa is connected between a redundant data line (RDL) and data input input/output line IO0. As described with reference to FIG. 1, Namekawa teaches that switches SW10 through SW115 and SW20 through SW215 are connected in such an arrangement, as shown in FIG. 1, to allow Namekawa to replace a defective data line with another data line in a data line shift method taught by Namekawa. Applicant cannot find in Namekawa a teaching or

fair suggestion that switches SW10 through SW115 and SW20 through SW215 of Namekawa can be arranged or connected in series with a memory segment between a supply node and an internal node of the device of Namekawa. In contrast, claim 13 recites that each of the switching units is connected “in series with one of the memory segments between the second supply node and one of the internal nodes”.

Namekawa also teaches, in FIG. 1, decode circuits D0 through D15 in which switches SW10 through SW115 and SW20 through SW215 (discussed above) receive output signals from decode circuits D0 through D15 to replace a defective data line with another data line. Applicant cannot find in Namekawa a teaching or fair suggestion that that switches SW10 through SW115 and SW20 through SW215 are used by Namekawa to disconnect a memory segment from a supply node based on the states of the output signals from decode circuits D0 through D15. In contrast, claim 13 recites that “each of the switching units includes an input node for receiving a select signal to electrically disconnect one of the memory segments from the second supply node based on a state of the select signal”.

Based on the reasons presented above, Applicant believes that claim 13 is patentable over Namekawa. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 13. Dependent claims 14-16 depend from claim 13 and recite the things of claim 13. Thus, Applicant believes that claims 14-16 are also patentable over Namekawa for at least the reasons presented above regarding claim 13, plus the additional things recited in claims 14-16. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 14-16.

Independent claim 48 recites, among other things, “a plurality of first switching units, each of the first switching units connecting in between the first supply node and one of the memory segments” and “a plurality of second switching units, each of the second switching units connecting between the second supply node and one of the memory segments”. For the reasons at least similar to those presented above regarding claim 13, Applicant cannot find in Namekawa a teaching or fair suggestion of “a plurality of first switching units, each of the first switching units connecting in between the first supply node and one of the memory segments” and “a plurality of second switching units, each of the second switching units connecting between the second supply node and one of the memory segments”.

Claim 48 also recites that each of the memory cells includes “a first storage node and a second storage node”. The Office Action compares memory cells of memory cell array 10 of Namekawa to the memory cells of claim 10. However, as shown in FIG. 1 of Namekawa, each of the memory cells in memory array 10 is a dynamic random access memory (DRAM) cell with only a single storage node at the capacitor CC in each DRAM cell. In contrast, claim 48 recites that each of the memory cells includes “a first storage node and a second storage node”.

Based on the reasons presented above, Applicant believes that claim 48 is patentable over Namekawa. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 48. Dependent claims 49-57 depend from claim 48 and recite the things of claim 48. Thus, Applicant believes that claims 49-57 are also patentable over Namekawa for at least the reasons presented above regarding claim 48, plus the additional things recited in claims 49-57. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 49-57.

Independent claim 58 recites, among other things, “a supply control circuit connected in the supply path for isolating a memory segment of the memory array from the supply node if the memory segment is defective”. The Office Action does not specifically point out where in Namekawa that teaches “a supply control circuit connected in the supply path for isolating a memory segment of the memory array from the supply node if the memory segment is defective”. Nevertheless, Applicant cannot find in Namekawa a teaching or fair suggestion of “a supply control circuit connected in the supply path for isolating a memory segment of the memory array from the supply node if the memory segment is defective”. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 58. Dependent claims 59-62 depend from claim 58 and recite the things of claim 58. Thus, Applicant believes that claims 59-62 are also patentable over Namekawa for at least the reasons presented above regarding claim 58, plus the additional things recited in claims 59-62. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 59-62.

Independent claim 63 recites, among other things, “isolating a memory segment of the memory device from a supply source if the memory segment is defective”. The Office Action does not specifically point out where in Namekawa that teaches “isolating a memory segment of

the memory device from a supply source if the memory segment is defective". Nevertheless, Applicant cannot find in Namekawa a teaching or fair suggestion of "isolating a memory segment of the memory device from a supply source if the memory segment is defective". Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 63. Dependent claims 64 and 65 depend from claim 63 and recite the things of claim 63. Thus, Applicant believes that claims 64 and 65 are also patentable over Namekawa for at least the reasons presented above regarding claim 63, plus the additional things recited in claims 64 and 65. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 64 and 65.

Claims 13, 48, 58 and 63 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Cleveland et al. (U.S. 5,349,558, hereinafter referred to as Cleveland).

Applicant respectfully traverses for at least the reasons presented below

The Office Action relies on FIG. 1 and a passage in column 4 lines 45-66 of Cleveland to reject claims 13, 48, 58 and 63 without specifically pointing out where in FIG. 1 and in the passage in column 4 lines 45-66 of Cleveland that everything recited in each of the claims 13, 48, 58 and 63 can be found. FIG. 1 of Cleveland teaches a chip layout for redundant blocks and sectors of array of EEPROM cells. The passage in column 4 lines 45-66 mainly describes FIG. 2 of Cleveland, which is a detailed schematic circuit diagram of the redundant blocks of FIG. 1 of Cleveland. Applicant cannot find in FIG. 1, in the passage in column 4 lines 45-66, or in the entire teaching of Cleveland, everything recited in each of the claims 13, 48, 58 and 63.

Regarding claim 13, Applicant cannot find in Cleveland a teaching or fair suggestion of the things recited in claim 13 such as "a plurality of switching units, each of the switching units connecting in series with one of the memory segments between the second supply node and one of the internal nodes" and "each of the switching units includes an input node for receiving a select signal to electrically disconnect one of the memory segments from the second supply node based on a state of the select signal".

Regarding claim 48, Applicant cannot find in Cleveland a teaching or fair suggestion of the things recited in claim 48 such as "a plurality of first switching units, each of the first switching units connecting in between the first supply node and one of the memory segments", "a plurality of second switching units, each of the second switching units connecting between the

second supply node and one of the memory segments”, and “each of the memory cells includes a first storage node and a second storage node”.

Regarding claim 58, Applicant cannot find in Cleveland a teaching or fair suggestion of the things recited in claim 58 such as “a supply control circuit connected in the supply path for isolating a memory segment of the memory array from the supply node if the memory segment is defective”.

Regarding claim 63, Applicant cannot find in Cleveland a teaching or fair suggestion of the things recited in claim 63 such as “isolating a memory segment of the memory device from a supply source if the memory segment is defective”.

Based on the reasons presented above, Applicant believes that claims 13, 48, 58 and 63 are patentable over Cleveland. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 13, 48, 58 and 63.

New Claims

Applicant believes that new claims 76-78 are patentable over the cited art. Accordingly, Applicant requests consideration and allowance of new claims 76-78.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6969 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

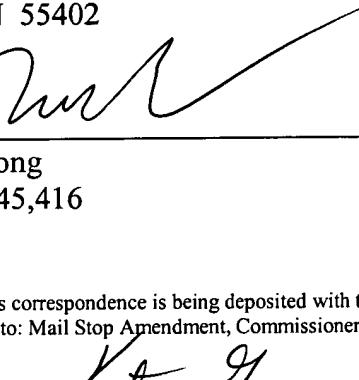
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Date 28 September 2006

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 28 day of September 2006.

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